VivaScope® AGC Disclosure

3/17/2000

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This document presents a method of measuring key image parameters for the purpose of automatically controlling laser intensity of a confocal imaging microscope, such as Lucid's VivaScope®, so as to provide optimally illuminated images.

Background

Lucid's VivaScope® and confocal imaging microscopes in general, use confocal imaging techniques to vertically section and image a tissue specimen. A raster scanned laser spot illuminates the in-focus specimen plane. Refracted light from the in-focus plane is converted to an electrical signal, digitized using a conventional high-speed A/D converter and displayed on a computer monitor as a 2-dimensional image.

Image intensity is both a function of imaging depth and specimen absorption characteristics. In normal VivaScope® operation, both are user controlled thereby requiring continuous laser power adjustment to maintain acceptable image brightness.

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This application discloses a means of monitoring key image parameters and effecting automatic laser power adjustment so as to maintain optimal image quality.

The notion of varying illuminating source intensity so as to maintain constant received signal strength, is routinely done in a variety of systems and devices, bar-code scanners for instance. This invention shows how the concept is applied to 2-dimensional images and confocal microscopy, and shows a practical implementation of same.

Description of Invention

Figure 1 shows one possible circuit to measure image brightness. The electronics are primarily digital in nature with exception of the analog video input buffer and development of an optional analog laser intensity control output (discusses below). The VivaScope® produces a ground referenced, DC coupled analog luminescence signal. Analysis of this signal is pivotal to adjusting image brightness.

Programmable logic such as is commonly available from companies such as the Xilinx® and Altera® implements this design allowing maximum algorithm flexibility. The two implementations discussed herein should not be taken in a limiting sense. As we become more experienced with the

behavior of the system many other algorithms for detecting image parameters to be controlled will become apparent.

For both circuits (Figure 1 & 2) image brightness control is based on two underlying assumptions: 1) if more than 12.5% (1/8' th) of the image' s total pixels are near saturation the image is too bright; 2) if more than half of the image' s pixels are near absolute black the image is too dark. Figure 2 differs from Figure 1 with the addition of circuitry to examine a rectangular window within the display area. Thus a means of ignoring display fringe areas that may be affected by optical distortion and not necessarily represent an accurate representation of the image is demonstrated. Further, it should be obvious to those skilled in the art that a simple averaging function can be applied over all pixels in the image or bounding rectangle (in the case of Figure 2) to yield a single numeric value.

Circuit Description (Figure 1)

The VivaScope' s analog video signal is buffered by amplifier A1 and fed into analog-to-digital converter ADC1. The buffer amplifier is included to prevent this circuit from adding noise to the video signal that is also supplying the main display (***frame-grabber*** PCB in a personal computer, not shown).

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A/D conversion is synchronized to the VivaScope's pixel clock (PCLK). Each digitized pixel is compared with two values, 10 and 250, representing ***DIM*** and ***BRIGHT*** threshold values, respectively. The comparisons are performed by digital comparitors CP2 and CP1, respectively. The DIM and BRIGHT values might be known ahead of time, as is the case for this example, or they be loaded by the host computer during operation.

Counters CN1-CN3 count the number of *bright, dim and total* pixels in a frame. Once each frame, as defined by the VivaScope's frame clock (VSYNC), the number of bright pixels is compared to 1/8'th of the total number of pixels (12.5%) the output of divider circuit DIV1[1], and the number of dim pixels is compared to _ the total pixels (50%), the output of DIV2, by CP3 and CP4, respectively. If 12.5% of the frame's pixels are bright and more than 50% are not dim, the LASER_DOWN signal is asserted by AND1. Conversely, if more than 50% of pixels are dim and less than 12.5% are bright, LASER_UP is asserted by AND2. If neither of these two conditions is satisfied neither LASER_UP or LASER_DOWN is asserted. Flip-flop FF1 generates a time-window indicating when the latched counter outputs are valid for comparison, between pixels 8 and 1024 of a frame. The first value is large enough to insure latches LA1-3 are stable, the second

value is large enough so the overall gate width of FF1 is sufficient for external circuitry.

These two output signals, LASER_UP and LASER_DOWN, are monitored by the VivaScope® controller that adjusts laser power by fixed, but not necessarily equal amounts, in the indicated direction. Alternately, laser control is performed locally using the optional analog laser control output named *Analog laser control.* This signal provides an analog output voltage whose amplitude is proportional to desired laser operating power. Its operation is learned from many common phase comparitor pump circuits used in PLLs. The LASER_DOWN signal activates the enable signal of a three-state buffer ZBUF1. ZBUF1 discharges C1 through R2. Conversely, the LASER_UP signal enables three-state buffer ZBUF2 allowing C1 to charge to the supply voltage through R1. The time-constants formed by C1-R1, and C1-R2 determine the system response, and hence the control loop response characteristics. The output must be buffered to prevent leakage current from significantly affecting C1's charge.

The circuit of Figure 1 cannot perform proportional control because its correction interval is fixed by the duration of FF1's high-time. It is not difficult to imagine alternate schemes whereby the outputs of LA1 and LA2 are multiplied by a convenient constant, such as 100, and then numerically

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[1] Care is taken in the design to require division only by integer powers of 2 so division is nothing more

divided by LA3 thus producing a varying value representing the percentage of BRIGHT and DIM pixels in each successive frame, respectively. The host computer, given the ability to retrieve these values[2], can implement proportional control.

Circuit Description (Figure 2)

The circuit shown in Figure 2 is an enhancement to Figure 1 with the addition of a rectangular region detector.

Counters CN4 and CN5 track the current pixel's position on the display. The digital edge detector circuits formed by FF2, FF3, XOR1 and AND4 produce a single pulse on the rising edge of HSYNC (e.g. the start of each scan line), thus resetting counter CN4. In this manner, CN4's count is always the pixel number in each scan line. Likewise, FF4, FF5, XOR2, and AND5 force CN5 to count the number of scan lines elapsed in the current frame. Digital comparitors CP5-8 compare the current pixel location (pixel and scan line) with registers REG1-4. These registers are loaded from the host computer with LEFT, RIGHT, TOP and BOTTOM values that define a screen rectangle defining the area of interest (AOI). When all comparitor outputs are simultaneously high, the beam is

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than comparing transposed bit values.

[2] Whether or not explicitly stated, it is assumed the host has the ability to retrieve and transmit key values to the circuitry described herein.

in the AOI as signaled by AND3's output activating. This signal effectively enables the circuit discussed above (Figure 1).